3rd national RISC-V student contest 2022-2023

Sponsored by Thales, the GDR SoC² and the CNFM

CV32A6 RISC-V soft-core hackathon

You are students and like new challenges.
You are interested in electronics, computer architectures and embedded cybersecurity.
You want to participate in the adventure of a renowned OpenHW processor core.
Then join this contest and win up to € 5,000!

Context

Thales is a world leader for mission critical information systems for the security, defense, space, aerospace and ground transportation domains. It employs 81,000 people in 68 countries. Following the success of two national RISC-V student contests (2020-2021, 2021-2022), Thales Research & Technology France, together with the GDR SOC² and the CNFM, are proud to announce the co-organization of the 3rd edition of the contest (2022-2023). This new contest will focus on the **security** of the CV32A6 RISC-V soft-core.

Targeted participants

Team of 1 to 4 **Master 2 students** or equivalent, registered in a **French engineering school or university** and coached by a **supervisor** (usually a teacher, assistant professor, professor…)

Planning

Main deadlines:

- Mid of October 2022: launch the contest (detailed rules and deadlines), start registering teams (until 2023-01-31). Students can start studying the technical topics (CV32A6, security…) before getting the technical kit.
- Beginning of November 2022: Thales releases the technical kit for the students.
- April-May 2023: deadline to submit results, defense sessions.
- June 2023: Prize ceremony

The detailed planning and deadlines will be announced when the contest is launched, in October 2022.

Prerequisites

The list of CAD tools and the FPGA board are unchanged w.r.t. the previous editions, so that schools/universities having participated last year may have the pre-requisite for this contest.

Because of the current tensions on supply chains, you should **anticipate as soon as possible the provisioning of the mandatory FPGA development environment** to avoid unnecessary delays. The list of necessary material is:

Reference	URL	Remark
Zybo Z7-20	https://store.digilentinc.com/zybo-z7-zynq-7000-arm-fpga-soc-development-board/	Zybo Z7-10 is too small for CVA6.
Pmod USBUART	https://store.digilentinc.com/pmod-usbuart-usb-to-uart-interface/	Used for the console output

JTAG-HS2 Programming Cable	https://store.digilentinc.com/jtag-hs2-programming-cable/	
Connectors	https://store.digilentinc.com/pmod-cable-kit-2x6-pin-and-2x6-pin-to-dual-6-pin-pmod-splitter-cable/	At least a 6-pin connector Pmod is necessary; other references may offer it.

Supervisors must **make sure the student teams will have this FPGA environment**. They can order the complete set from CNFM (contact: fpga@cnfm.fr).

Other prerequisites are Mentor Questa digital simulator (though CNFM license server) and Xilinx Vivado. The technical kit prepared by Thales will be developed on Linux Ubuntu 20.04.

Contacts

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